Art Unit: 2444

EXAMINER'S AMENDMENT

 An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Demort Miller (Reg. No. 58,309) on 6/29/2010.

Examiner Amendments

The application has been amended as follows:

- 1. (Currently Amended) A network interface of a host system, comprising:
- a direct memory access unit;
- a network data transmit path to couple [[a]] said host system to a network, the network data transmit path leading to the network; and circuitry to:
 - receive and transmit network data for a host processor of the host system, the transmitting of the network data being via the network data transmit path to the network:
 - intercept from among network data in the network data transmit path one or more packets received from said host processor;
 - generate, based on the receiving and transmitting network data, a set of statistics metering operation of the network interface, the set of statistics including

Art Unit: 2444

at least one selected from the group of: (1) a number of bytes received, and (2) a number of packets received;

periodically initiate direct memory access transfers of the set of statistics from the network interface to a memory of the host system accessible by the host processor,

wherein the circuitry to initiate the direct memory access transfers at a periodicity of a time interval value;

determine configuration information from a payload of said one or more packets,

wherein said circuitry to determine said configuration information from the

payload of said one or more packet identifies information in the one

or more packets indicating that the one or more packets are not to

be transmitted over the network;

wherein said configuration information comprises said time interval value;

configure said initiation of the direct memory access transfers using [[a]] said configuration information, wherein the circuitry to determine said configuration information from a payload of said one or more packets, wherein said configuration information comprises said time interval value.

(Previously Presented) The network interface of claim 1, wherein the set of statistics comprises each of the following: a number of packets received by the

Art Unit: 2444

interface, a number of bytes received by the interface, a number of packets transmitted by the interface, and a number of bytes transmitted by the interface.

- 3. (Previously Presented) The network interface of claim 2, wherein the circuitry comprises circuitry to include a timestamp with the direct memory access transfer of the set of statistics, the timestamp being a time when values of the set of statistics transferred by direct memory access were set by the network interface.
- 4. (Previously Presented) The network interface of claim 2, wherein the circuitry comprises circuitry to include a sequence count with the direct memory access transfers of the at least one statistic, the sequence count sequentially numbering successively DMA-ed sets of the statistic.
- (Previously Presented) The network interface of claim 1, wherein the set of statistics comprises multiple RMON (Remote Monitoring) statistics.
- (Previously Presented) The network interface of claim 1, wherein the circuitry comprises circuitry to initiate direct memory access transfer of received network data
- (Original) The network interface of claim 1, wherein the network interface comprises a framer.

Art Unit: 2444

8. (Original) The network interface of claim 7, wherein the network interface

comprises a Media Access Controller (MAC).

9. (Original) The network interface of claim 1, wherein the network interface

comprises a PHY.

Claims 10 and 11. (Canceled).

12. (Original) The network interface of claim 10, wherein the circuitry to configure

comprises at least one register.

13. (Previously Presented) The network interface of claim 1, wherein the circuitry

to configure comprises circuitry to determine from said configuration information

a first location in the memory for a first direct memory access transfer and a

second location in the memory, different from the first location, for a second

direct memory access transfer.

14. (Previously Presented) The network interface of claim 13, wherein the circuitry to

periodically initiate direct memory access transfers comprises circuitry to:

initiate the first direct memory access transfer based on the determining the first location, the first direct memory access transfer to transfer to the first location data indicating a first value of a statistic at a first time; and initiate, after the first direct memory access transfer, the second direct memory access transfer based on the determining the second location, the second direct memory access transfer to transfer to the second location data indicating a second value of the statistic at a second time.

15. (Original) The network interface of claim 1, wherein the direct memory access unit comprises circuitry to notify a processor of completion of a transfer.

Claims 16-38. (Canceled).

- 39. (Previously Presented) The network interface of claim 14, wherein the memory of the host system comprises a ring including the first location and the second location, the ring to store snapshots of counter values of the network interface.
- 40. (Previously Presented) The network interface of claim 14, wherein the first location is appended to a linked list after the first direct memory access transfer, and wherein the second location is appended to the linked list after the second direct memory access transfer.

Application/Control Number: 10/722,747

Art Unit: 2444

41. (Cancelled)

Reasons for Allowance

- The following is an examiner's statement of reasons for allowance:
- 3. US 6,434,620 to Boucher discloses a network interface, which collects statistics and transmits information via direct memory access. However, Boucher does not disclose at least the configuration of the network interface by sending a packet from the processor of the host system as network traffic, where information in the information in the packet indicating that the packet is not to be transmitted over the network, and where payload data in the packet includes the configuration information.
- 4. In 5,699,350, Kraslavsky discloses a packet that includes information for configuration of an interface (Kraslavsky: Abstract). However, Kraslavsky does not teach that the packet to configure the network interface of a system is sent from the processor of the system. Further, no other prior art of record fairly teaches or suggests modifying the teachings of Boucher to configure the network interface in the manner disclosed by claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Christensen whose telephone number is (571)270-1144. The examiner can normally be reached on Monday through Thursday 6:30AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Vaughn can be reached on (571) 272-3922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. C./

Examiner, Art Unit 2444 /William C. Vaughn, Jr./

Supervisory Patent Examiner, Art Unit 2444